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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,809	11/15/2001	Elizabeth A. Richard	COMP-0246 P01-3670	3825
7	590 03/24/2004		EXAMI	NER
Michael G. Fletcher PERVEEN, RE				REHANA
•	r & Van Someren		ART UNIT PAPER NUMBER	
P.O. Box 6922			ARI ONII	TATERNOVEER
Houston, TX	77269-2289		DATE MAILED: 03/24/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Applicati	on No	Applicant(s)			
Office Action Summary	10/002,8		RICHARD ET AL.			
Office Action Summary	Examine		Art Unit			
The MAIL INC DATE of this account	Rehana		2182			
The MAILING DATE of this communic Period for Reply	ation appears on the	e cover sheet with the c	correspondence address			
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed	1) Responsive to communication(s) filed on <u>15 November 2001</u> .					
2a) ☐ This action is FINAL. 2t	2a) ☐ This action is <b>FINAL</b> . 2b) ☑ This action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-46</u> is/are pending in the ap	plication.					
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-4, 7-14, 17-26, 29-43, and 46</u> is/are rejected.						
7)⊠ Claim(s) <u>5,6,15,16,27,28,44 and 45</u> is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the	Examiner.					
10)⊠ The drawing(s) filed on <u>15 November 2001</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim to	or foreian priority un	der 35 U.S.C. & 119(a)	u-(d) or (f)			
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Aiteach						
Attachment(s)  1) Notice of References Cited (PTO-892)		4) [] Internation 6	(DTO 440)			
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  Paper No(s)/Mail Date.						
3) Information Disclosure Statement(s) (PTO-1449 or PT	ro/sb/08)	5) Notice of Informal P	atent Application (PTO-152)			
Paper No(s)/Mail Date <u>2</u> .  U.S. Patent and Trademark Office		6) Other:				
PTOL-326 (Rev. 1-04)	Office Action Summa	ry	Part of Paper No./Mail Date 3			



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#### **DETAILED ACTION**

### Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 40 and 44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 40, line 4, it is unclear whether the phrase "store a request corresponding to a request" should read "store an index corresponding to a request" to match other presented independent claims. Correction or clarification is therefore required.

As to claim 44, line 5, it seems that the phrase "the entry read flag" should read "the entry ready flag". Correction is therefore required.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 7-14, 18-26, 30-43, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al. Patent No. 6,356,972.

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As to claim 40, Chin et al teach a queue entry pool comprising a plurality of fixed registers configured to store requests (figure 4, queues 66 or 68), and an entry shifter coupled to the queue entry pool (figure 4, In-Order queue 64) and comprising a plurality of registers, each of the registers is configured to store a request corresponding to a request stored in one of the plurality of fixed registers (col. 5 lines 35-65 and col. 11 line 9 – col. 12 line 67).

However, Chin et al do not expressly teach the entry shifter registers being shift registers. It would have been obvious for one of ordinary skill in the art at the time of the invention to modify teachings of Chin et al to utilize such well known shift registers so that the system may perform entry shifting in an efficient manner.

As to claims 2, 9, 21, and 41, Chin et al teach the queue entry pool is configured to store read requests (col. 13 lines 14-29).

As to claims 3, 13, 25, and 42, Chin et al teach each of the plurality of fixed registers is configured to store a plurality of flags corresponding to the status of each request (col. 11 lines 9-62).

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As to claims 4, 14, 26, and 43, Chin et al teach each of the plurality of fixed registers is configured to store each of a valid entry flag, an entry ready flag, and a retire entry flag for the corresponding request (inherent, col. 11 lines 9-62).

As to claims 7 and 46, Chin et al teach a queue structure depth checker coupled to the queue entry pool and configured to track the number of requests stored in the queue (comparator, col. 5 line 46 – col. 6 line 7).

As to claim 1, Chin et al teach all of the limitations as stated above in claim 40. In addition, Chin et al teach each entry shifter register corresponds to one of the plurality of fixed registers (col. 11 lines 9-62).

As to claim 8, Chin et al teach all of the limitations as stated above in claims 40 and 1. In addition, Chin et al teach a plurality of processor controller interfaces configured to receive requests from one of a processor bus and an I/O bus, each request having a corresponding request type, and a plurality of queues coupled to each of the processor controller interfaces and configured to store requests, wherein each request is delivered to one of the plurality of queues depending on the origin of the request and the request type (figure 4, lines 9-24).

As to claims 10 and 22, Chin et al teach the plurality of queues comprises a plurality of write queues configured to store write requests (col. 13 lines 14-29).

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As to claims 11 and 23, it is noted that Chin et al do not expressly teach the plurality of queues being a plurality of IRV queues configured to store requests associated with a hot-plug event. However, Chin et al teaches storing requests in a queue based on the type of the request (figure 4). It would have been obvious for one of ordinary skill in the art at the time of the invention to recognize a specific type request such as the one associated with a hot-plug event and utilize specific type queues such as IRV queues since the advantages and benefits of using such has been quite well known in the prior existing queuing systems.

As to claims 12 and 24, Chin et al do not expressly teach generating and storing each of initialization requests, rebuild requests, and verify requests, each of the requests being generated in response to a hot-plug event. However, a routineer in the data processing art would have readily recognized that generation and storage of such requests responsive to a hot-plug event has been quite well known in the prior art at the time of the applicant's claimed invention.

As to claims 18 and 30, Chin et al teach a control block coupled to each of the plurality of queues and configured to provide control signals to facilitate the storing and execution of the requests in the plurality of queues (figure 4, col. 11 lines 9-36).

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As to claims 19 and 31, Chin et al teach a control interface block coupled to the control block and further coupled to each of the plurality of processor controller interfaces, wherein the control interface block is configured to transfer the requests from the plurality of processor controller interfaces to the control block (figure 4, col. 11 lines 9-36).

As to claim 20, Chin et al teach all of the limitations as stated above in claims 1 and 8. In addition, Chin et al teach one or more processors and a memory controller coupled to the one or more processors (col. 7 lines 23-34).

As to claim 32, Chin et al teach the system comprises a computer system (Computer 10, figure 1).

As to claim 33, Chin et al do not expressly teach the system comprising a network of computers. However, a routineer in the data processing art would have readily recognized that Chin et al's request queuing system within a computer could be extended to multiple computers within a network to enable the networked computers to efficiently utilize the advantages and benefits of the improved queuing system.

Claims 34-39 are directed to the method of system claims 1-4, 7-14, 18-26, 30-43, and 46. Chin et al teach the system as set forth in claims 1-4, 7-14, 18-26, 30-43, and 46. Therefore, Chin et al also teach the method as set forth in claims 34-39.

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Claims 17 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al, Patent No. 6,356,972, in view of Schrofer, Patent No. 4,682,284.

As to claims 17 and 29, Chin et al do not expressly teach a bypass block coupled to each of the plurality of processor controller interfaces and configured to facilitate the execution of the requests without storing the requests in one of the plurality of queues. Schrofer teaches a bypass block coupled to a controller interface and configured to facilitate the execution of requests without storing the requests in a queue (figure 3, abstract, and col. 1 lines 43-55). It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Chin et al and Schrofer because Schrofer's bypassing the queue mechanism, when incorporated into Chin et al's requests processing system, would have enabled the overall system to achieve an increased throughput by directly executing the request without storing when the queue is empty and the apparatus is ready to receive a request.

## Allowable Subject Matter

Claims 5, 6, 15, 16, 27, 28, 44, and 45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rehana Perveen whose telephone number is 703-305-.

8476. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey C Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Rehana Perveen

Primary Patent Examiner Technology Center 2100